



MS-7642 VER:10

CPU:

AMD AM3 (HT 3.0)

System Chipset:

AMD/ATI RS880D

AMD/ATI SB850

On Board Chipset:

FINTEK Super I/O -- F71889

LAN -- RTL8111DL

HD Codec -- ALC889

USB3.0 -- NEC uPD720200

PATA -- JMICRON JMB368

BIOS -- SPI ROM 8M

Main Memory:

DDR III X 4 (Max 8GB)

Expansion Slots:

PCI-E X 16 *2

PCI-E X 1 *1

PCI 2.2 Slot X 1

Clock Generator:

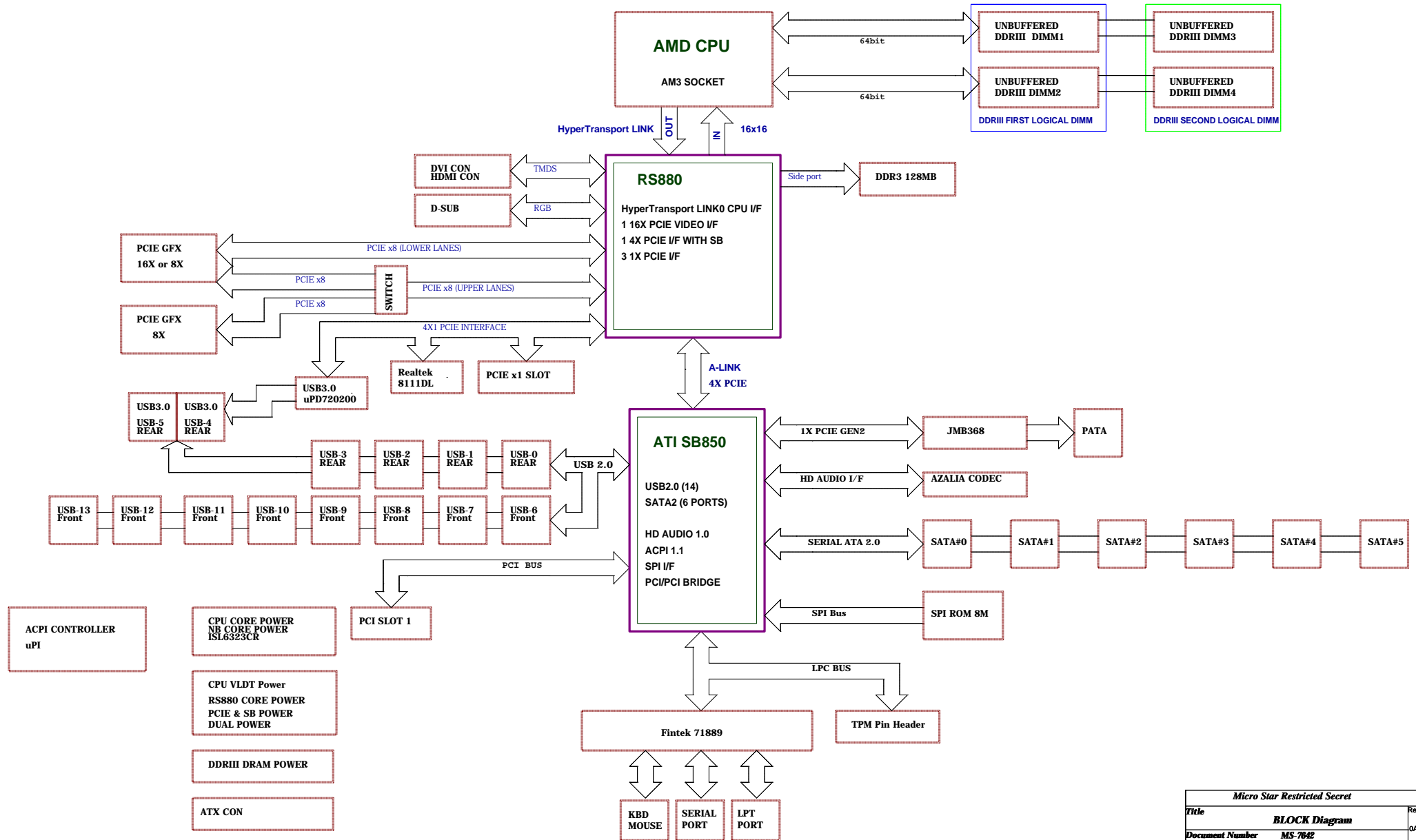
Controller--REALTEK RTM880N-793

PWM:

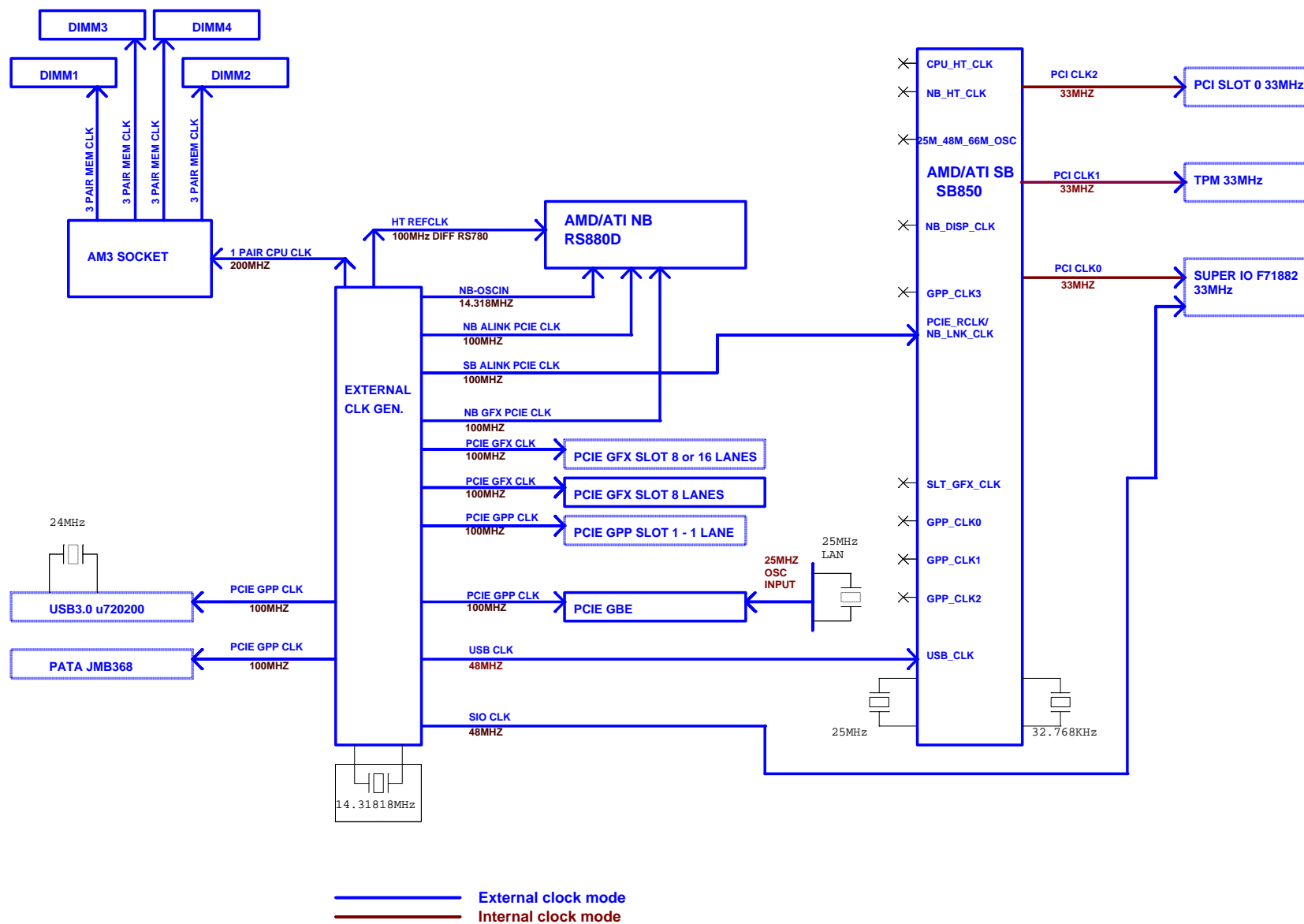
ISL6323+ISL6212

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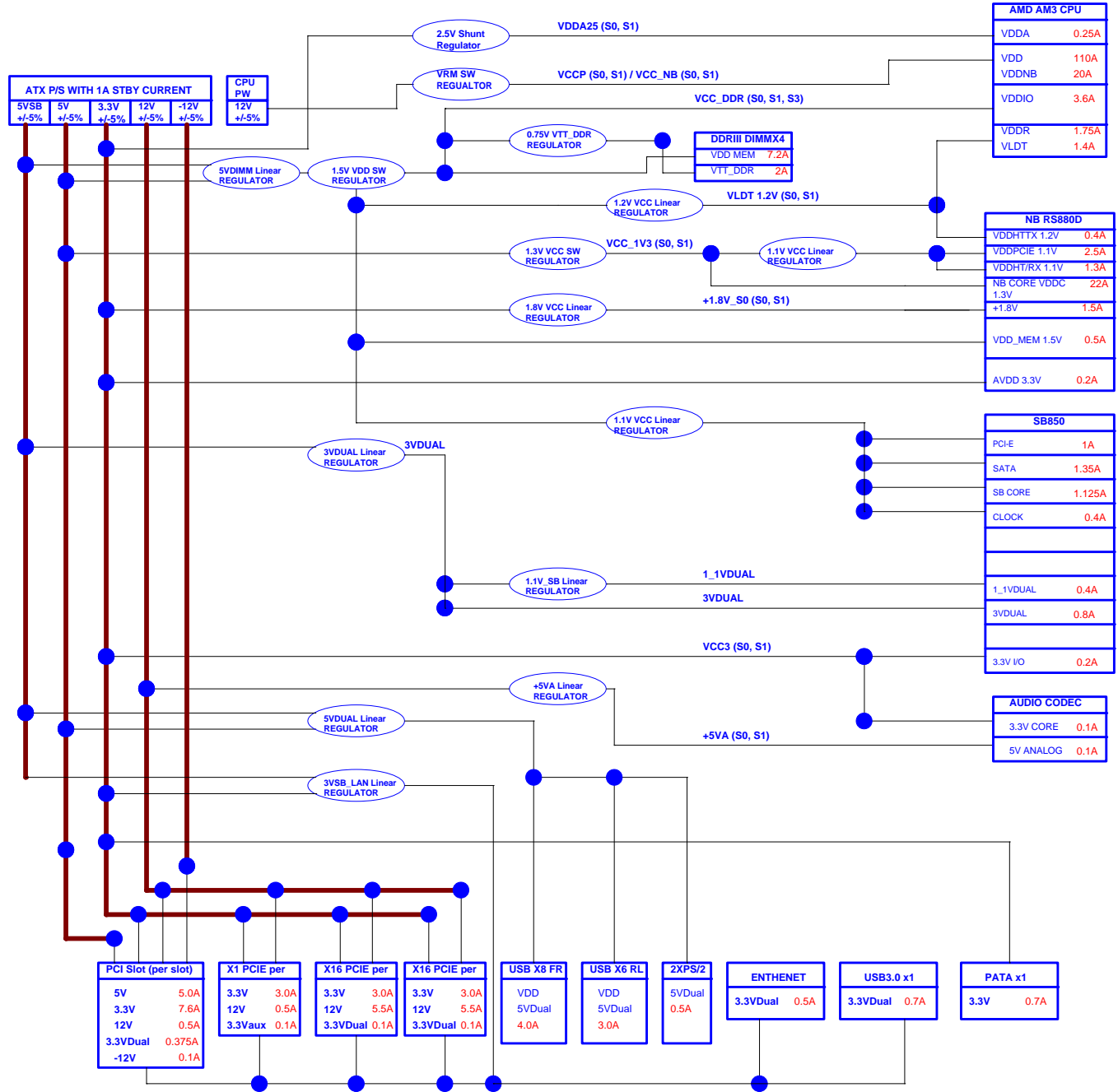
Project RS-880D BLOCK DIAGRAM



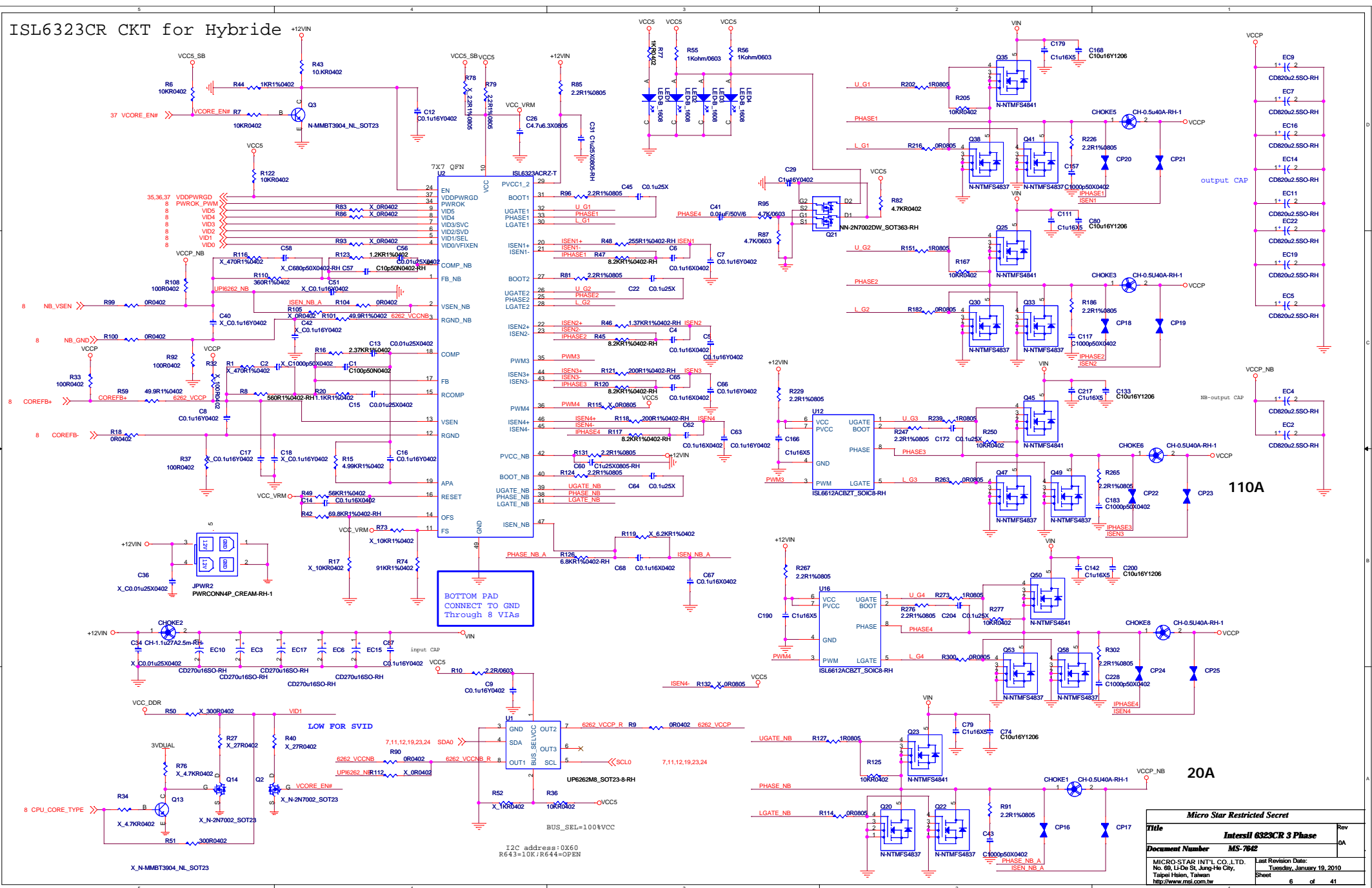
SB850 GPIO Config				
GPIO Name	Type	Function description	Pin	Page
GA20IN/GEVENT0#	I	GA20IN		
PCI_PME#/GEVENT3#	I	LPC_PME#		
LPC_PME#/GEVENT4#	I	PCIPME#		
WAKE#/GEVENT8#	I	WAKE#		
USB_OC0#/GEVENT12#	I	USB_OC0#		
USB_OC1#/GEVENT13#	I	USB_OC1#		
SYS_RESET#/GEVENT19#	I	SYS_RESET#		
SERIRQ/GPIO48	I/O	SERIRQ		
GPIO50	I	DUALX8_EN#		
SATA_ACT#/GPIO67	O	SATA_ACT#		
TALERT#/GPIO174	I	TALERT#		



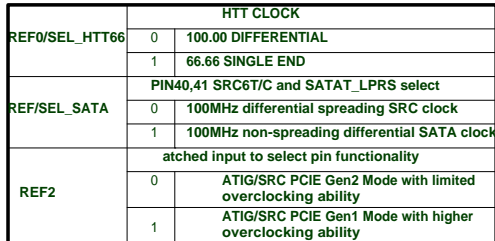
Power Deliver Chart

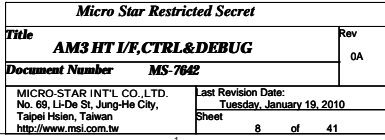


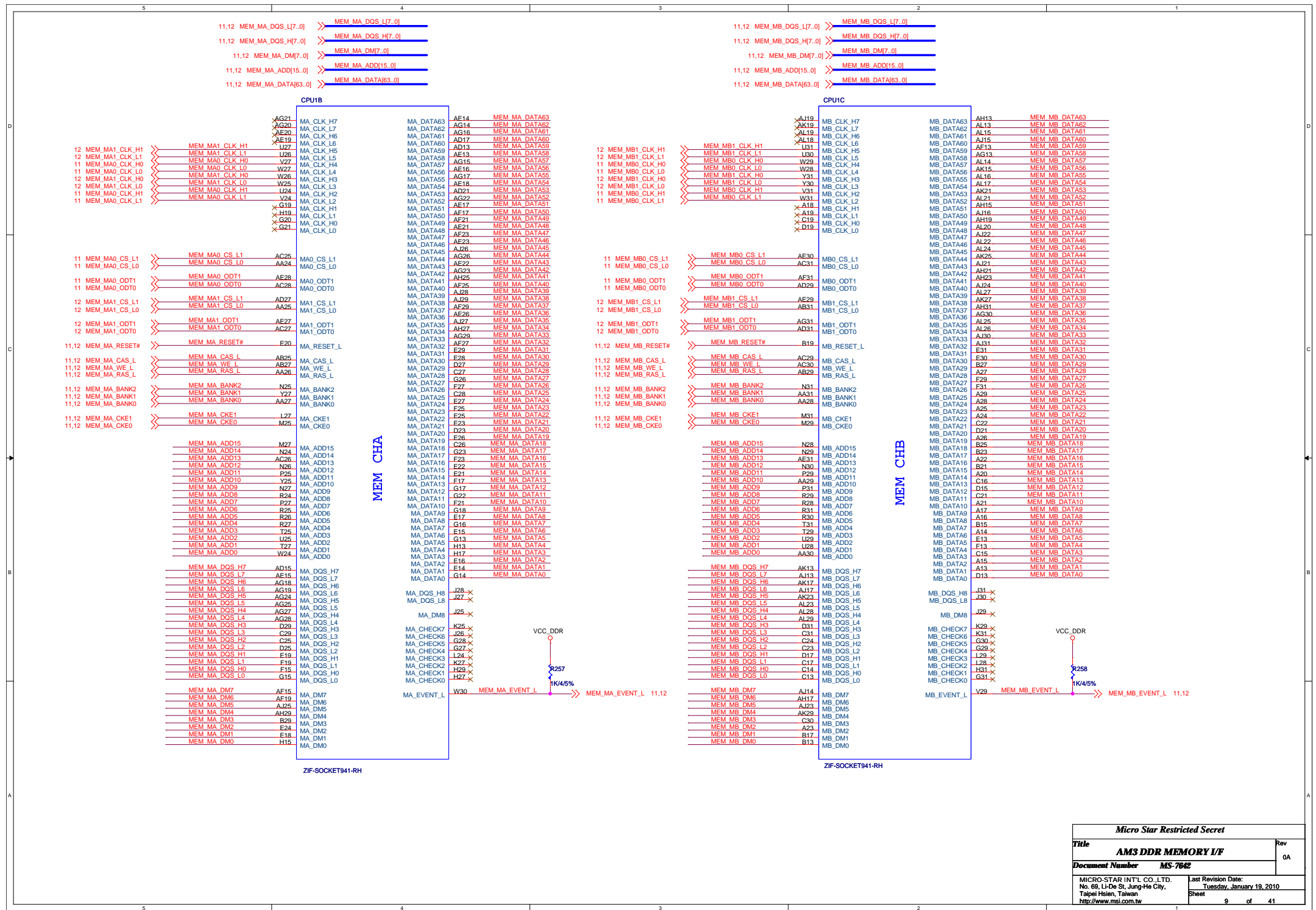
ISL6323CR CKT for Hybride

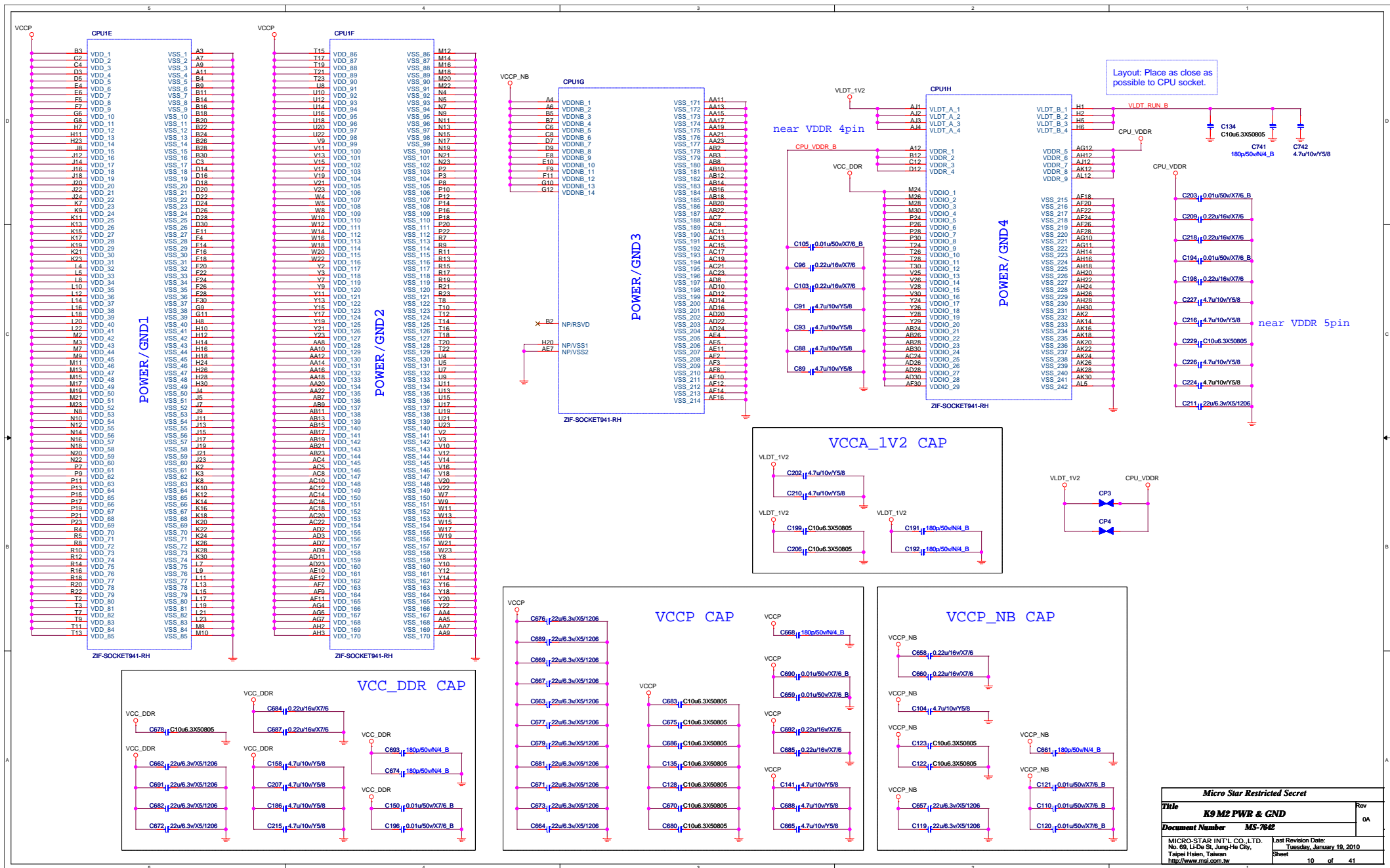


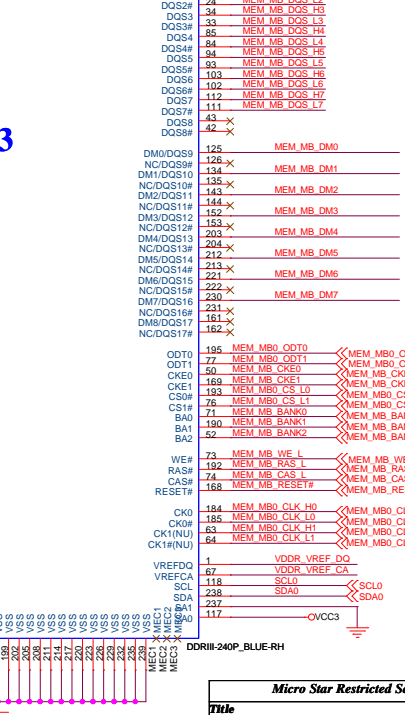
Micro Star Restricted Secret		
Title	Intersil 6323CR 3 Phase	Rev
Document Number	MS-7642	0A
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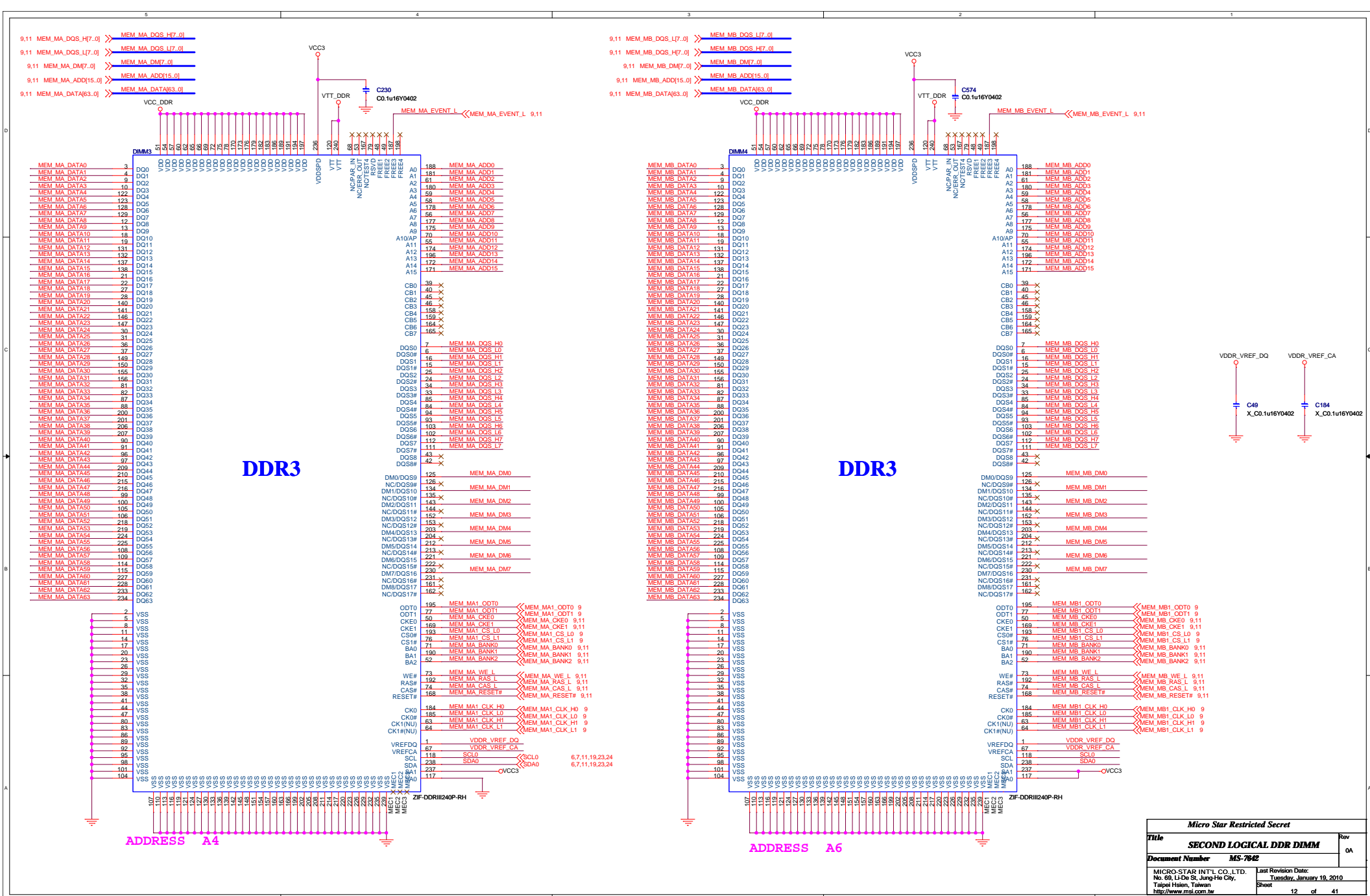


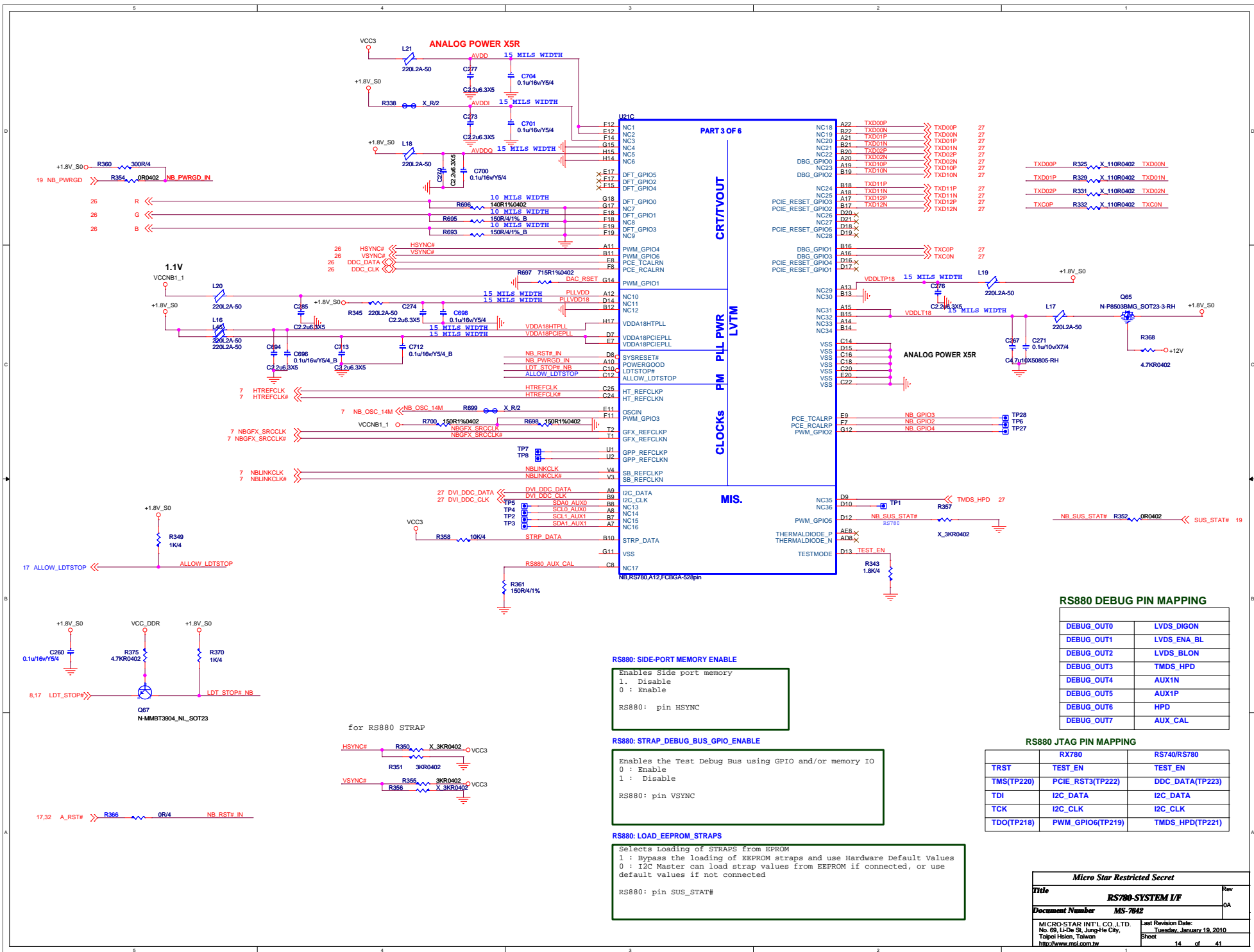












RS880 DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL

RS880 JTAG PIN MAPPING

TRST	RX780	RS740/RS780
TMS(TP220)	TEST_EN	TEST_EN
TDI	PCIE_RST3(TP222)	DDC_DATA(TP223)
TCK	I2C_DATA	I2C_DATA
TDO(TP218)	I2C_CLK	I2C_CLK
	PWM_GPIO6(TP219)	TMDS_HPD(TP221)

RS880: SIDE-PORT MEMORY ENABLE

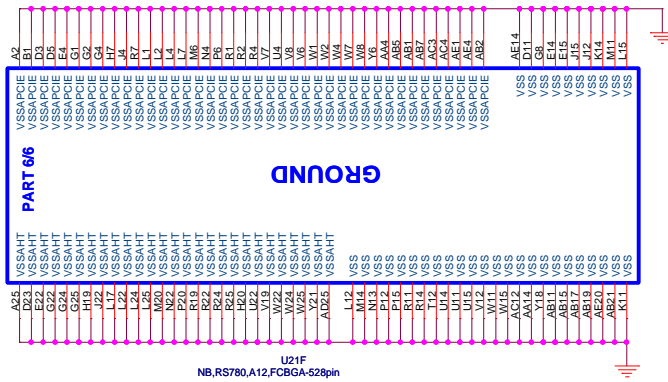
Enables Side port memory
1: Disable
0: Enable
RS880: pin HSYNC

RS880: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
0: Enable
1: Disable
RS880: pin VSYNC

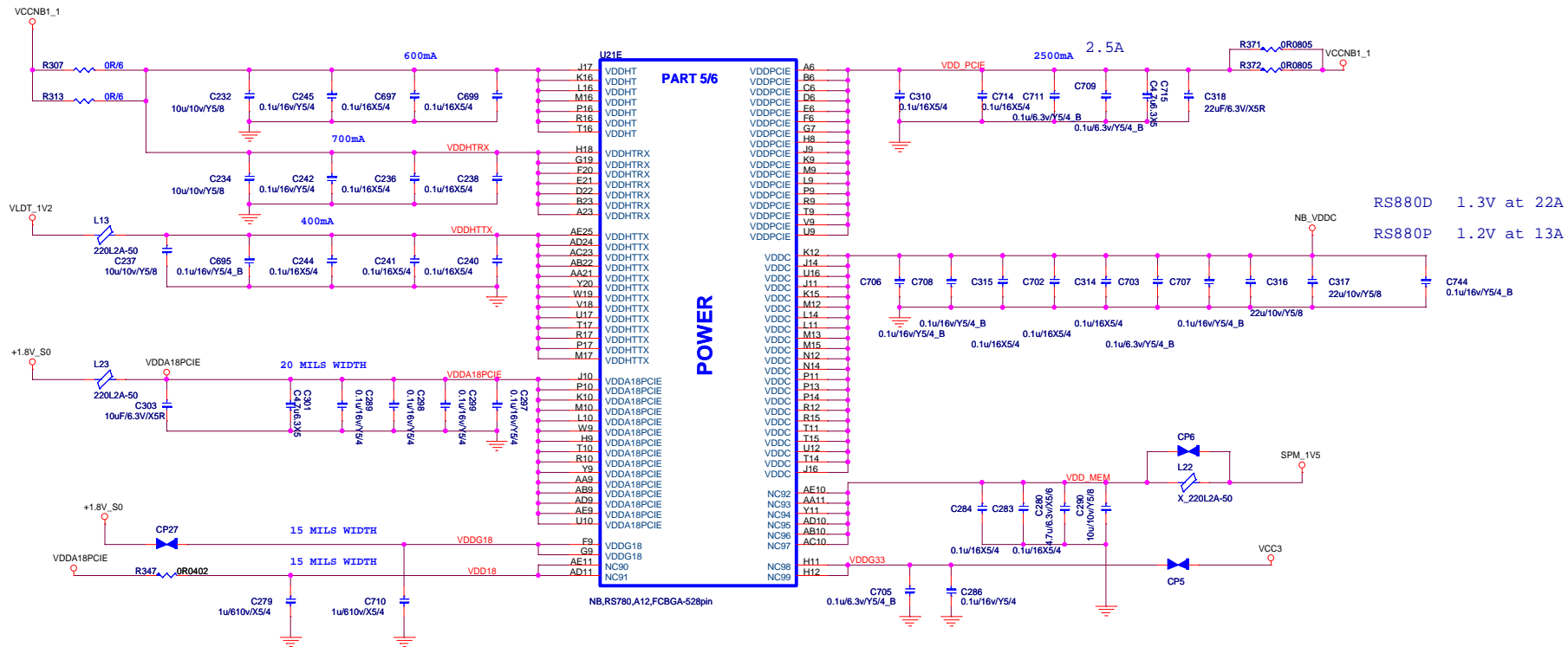
RS880: LOAD_EEPROM_STRAPS

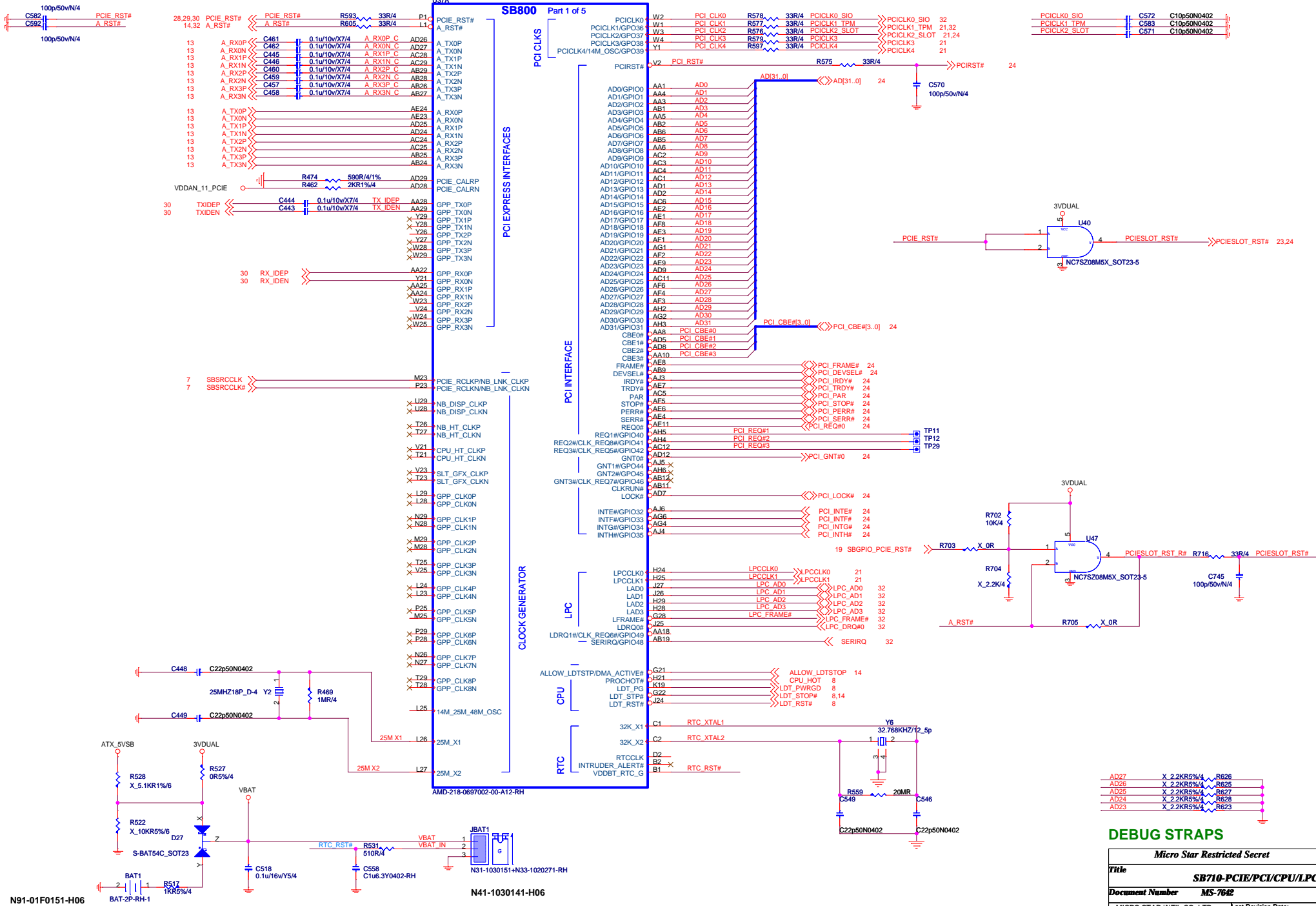
Selects Loading of STRAPS from EPROM
1: Bypass the loading of EEPROM straps and use Hardware Default Values
0: I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS880: pin SUS_STAT#



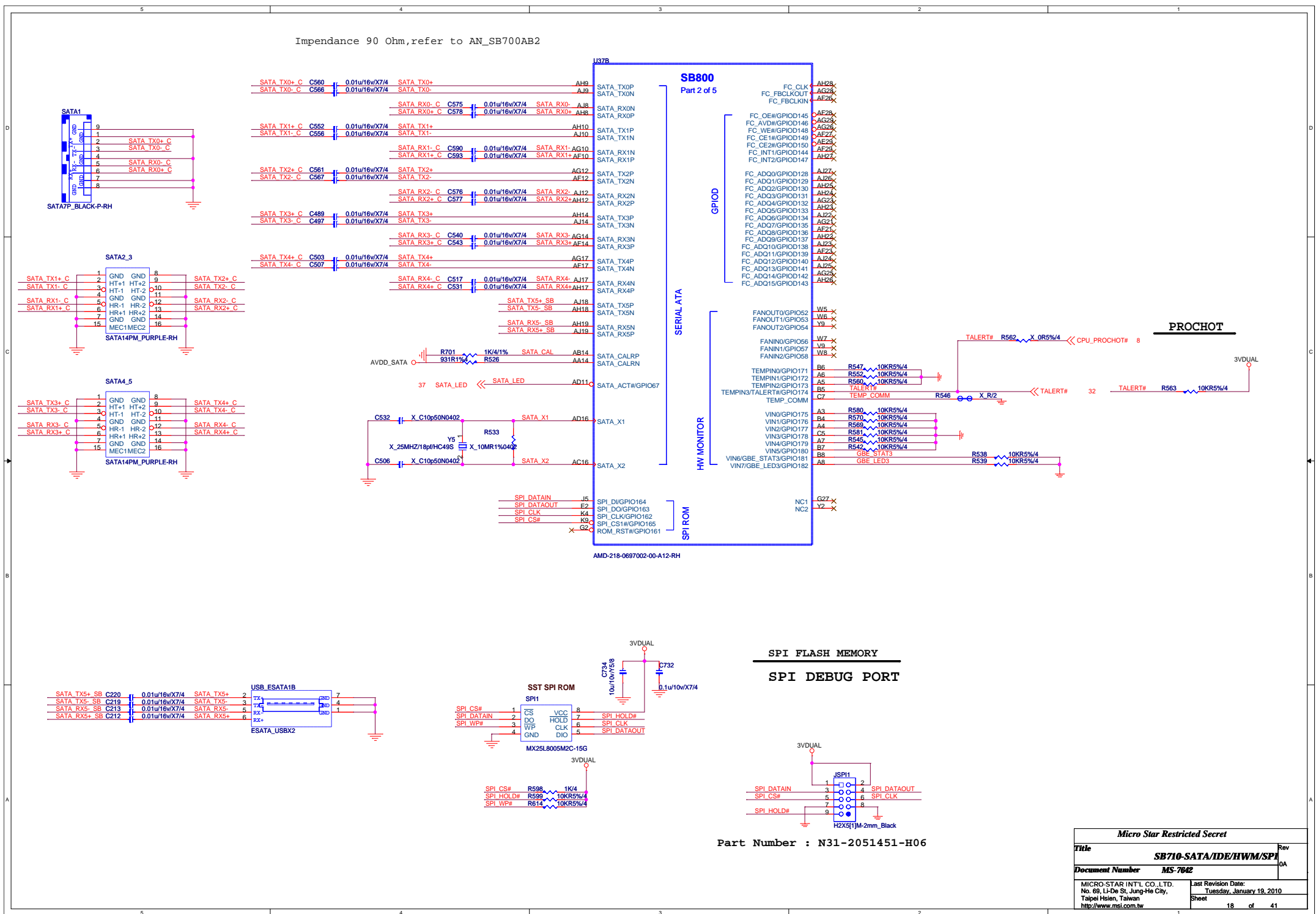
RS880D POWER TABLE

PIN NAME	RS780	PIN NAME	RS780
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDD18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.3V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.5V	VDDLTP18	+1.8V
VDD33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC





DEBUG STRAPS		
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PCI_PME# internal pull high 10k to 3V

24,32 PCI_PME# >> PCI PME# R566 X 0R5%/4 SB PME#

29,32,34,37 SLP_S3# << SLP_S3#
29,32,34,36 SLP_S5# << SLP_S5#
32 PWRBTN# << SB_PWRBTN#
37 SB_PWRGD << SB_PWRGD
14 SUS_STAT# << SUS_STAT#

32 A20GATE << A20GATE
32 KBRST# << KBRST#
32 LPC_PME# << LPC_PME#

7,37 FP_RST# << FP_RST#
23,24,28,29,32 PE_WAKE# << PE_WAKE#

8 CPU_THRIP# << CPU_THRIP#
14 NB_PWRGD << NB_PWRGD

32 RSMRST# << RSMRST#

22,23 DUALX8_EN# << DUALX8_EN#

37 SPKR << SPKR

15 SPM_RESET# << SPM_RESET#

7 SB_OSC_14M << SB_OSC_14M

17 SBGPIO_PCIE_RST# << SBGPIO_PCIE_RST#

25 USB_OCP#1 << USB_OCP#1
25,29 USB_OCP#0 << USB_OCP#0

31 AZ_BITCLK << AZ_BITCLK
21,31 AZ_SDOUT << AZ_SDOUT

31 AZ_SDIN0 << AZ_SDIN0

31 AZ_SYNC << AZ_SYNC
31 AZ_RST# << AZ_RST#

31 AZ_SYNC << AZ_SYNC
31 AZ_RST# << AZ_RST#

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31 AZ_SYNC << AZ_SYNC
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31 AZ_SYNC << AZ_SYNC
31 AZ_RST# << AZ_RST#

AMD-218-0697002-00-A12-RH

SB800
Part 4 of 5

ACPI / WAKE UP EVENTS

USB 1.1 USB MISC

USB 2.0

GPIO

USB OC

HD AUDIO

GBE LAN

EMBEDDED CTRL

EMBEDDED CTRL

EMBEDDED CTRL

EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC

USB_RCOMP

USB_FSDP/GPIO186

USB_FSDN

USB_FSDOP/GPIO185

USB_FSDON

USB_HSD13P

USB_HSD13N

USB_HSD12P

USB_HSD12N

USB_HSD11P

USB_HSD11N

USB_HSD10P

USB_HSD10N

USB_HSD9P

USB_HSD9N

USB_HSD8P

USB_HSD8N

USB_HSD7P

USB_HSD7N

USB_HSD6P

USB_HSD6N

USB_HSD5P

USB_HSD5N

USB_HSD4P

USB_HSD4N

USB_HSD3P

USB_HSD3N

USB_HSD2P

USB_HSD2N

USB_HSD1P

USB_HSD1N

USB_HSDOP

USB_HSDON

USB_HSDOP

USB_HSDON

USB_HSDOP

USB_HSDON

USB_HSDOP

USB_HSDON

USB_HSDOP

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USB_HSDOP

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USB_HSDON

USB_HSDOP

USB_HSDON

GPIO200 GPIO199

ROM TYPE: H, H = Reserved

H, L = SPI ROM

L, H = LPC ROM

L, L = FW ROM

DEFAULT

90 Ohm

3VDUAL

3VDUAL

R515 X 2.2K5%/4

R518 X 2.2K5%/4

GPIO199

GPIO200

R516 2.2K5%/4

R519 X 2.2K5%/4

GPIO199

GPIO200

GPIO199

GPIO200

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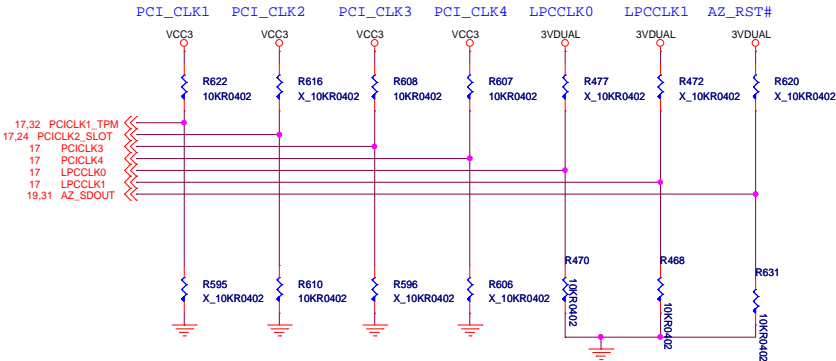
GPIO200

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SB710-ACPI/GPIO/USB/AUDIO		0A
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

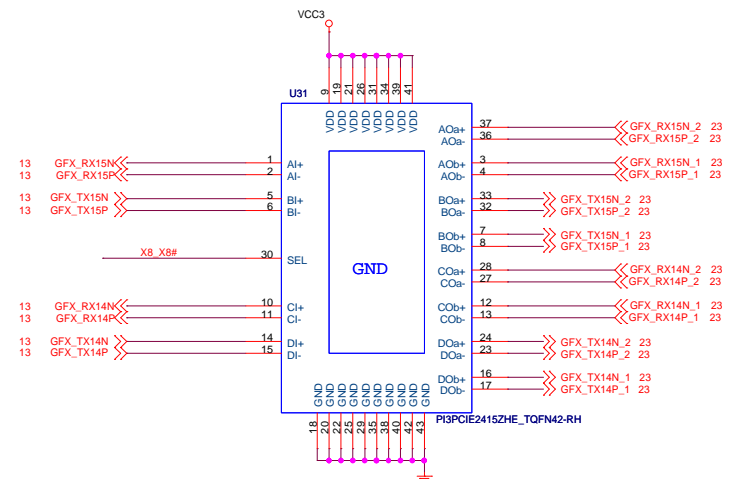
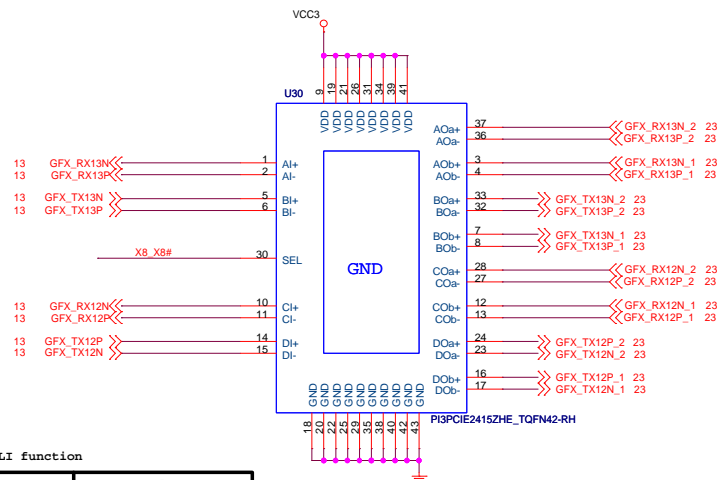
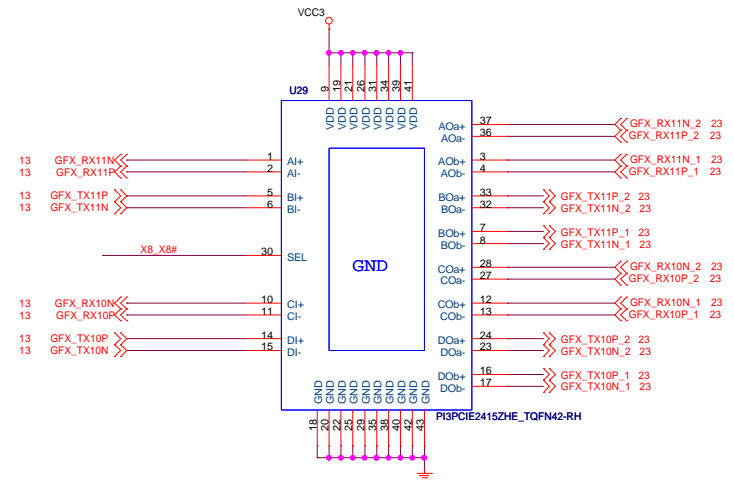
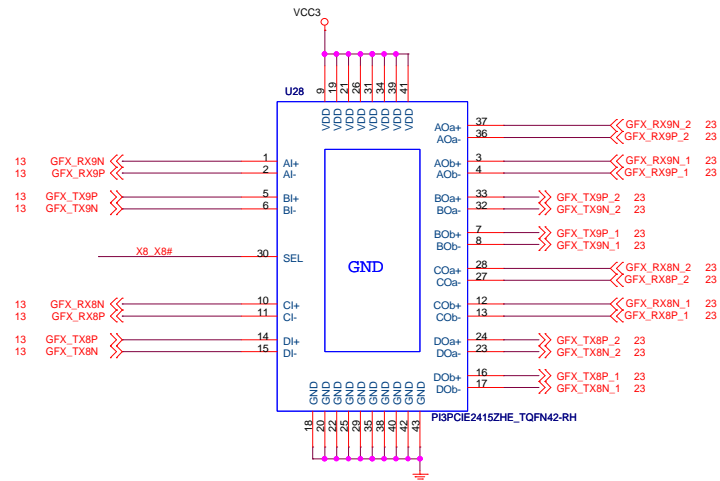


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	
PULL HIGH	CoreSpeedMode Low Power mode	PCIE at GEN2 mode DEFAULT	Watchdog timer Enable	Enable Debug Straps DEFAULT	Reserved DEFAULT	EC ENABLE	Integrated clock mode	
PULL LOW	CoreSpeedMode Performance mode DEFAULT	PCIE at GEN1 mode	Watchdog timer Disable DEFAULT	Disable Debug Straps	Reserved	EC DISABLE DEFAULT	External clock mode DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

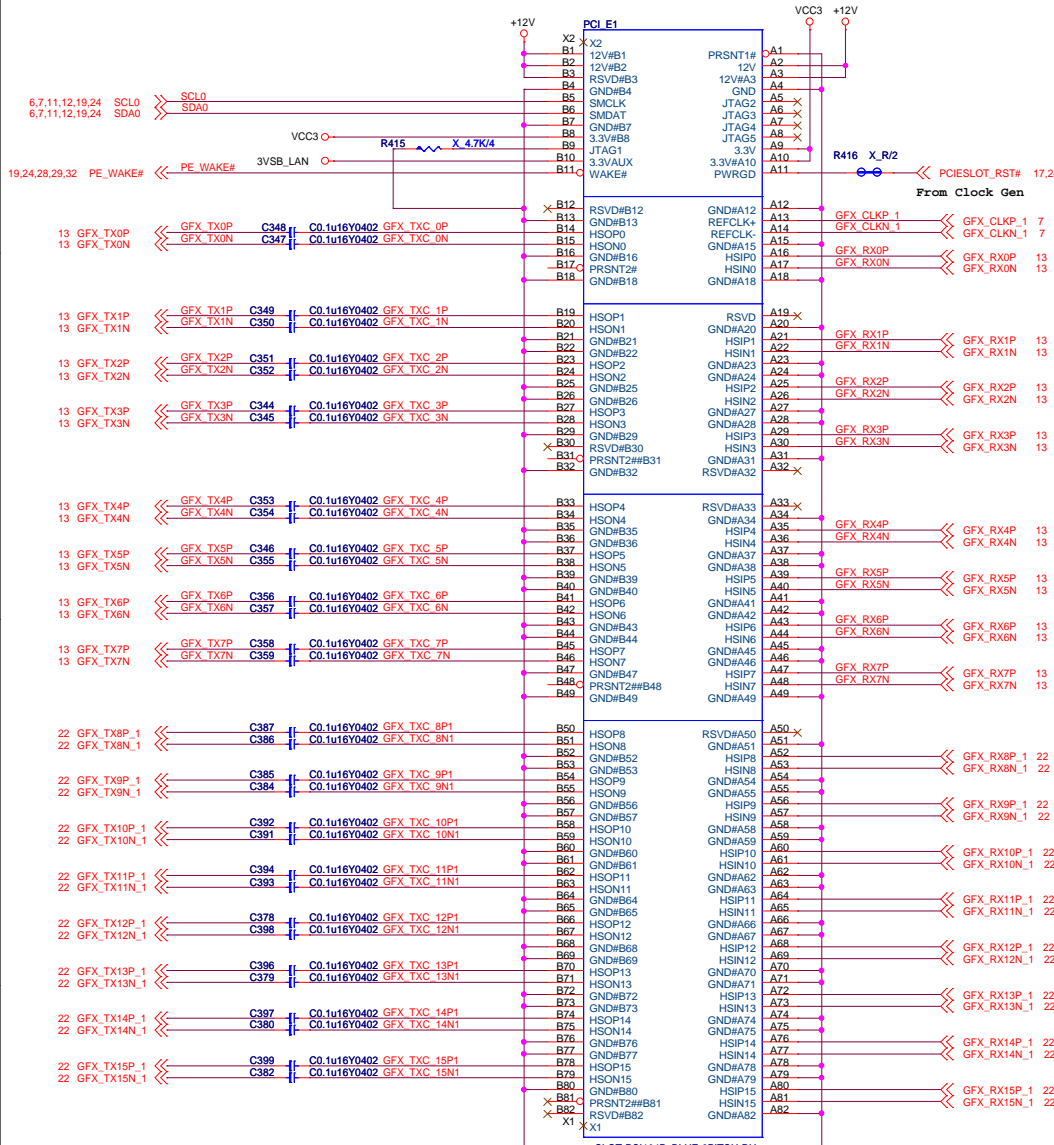


Digital Switch
SEL pin SLI function

DualX8_En#	Output	X8_X8	PCI-E_Slot 1/2
1	b	1	X16
0	a	0	X8 / X8

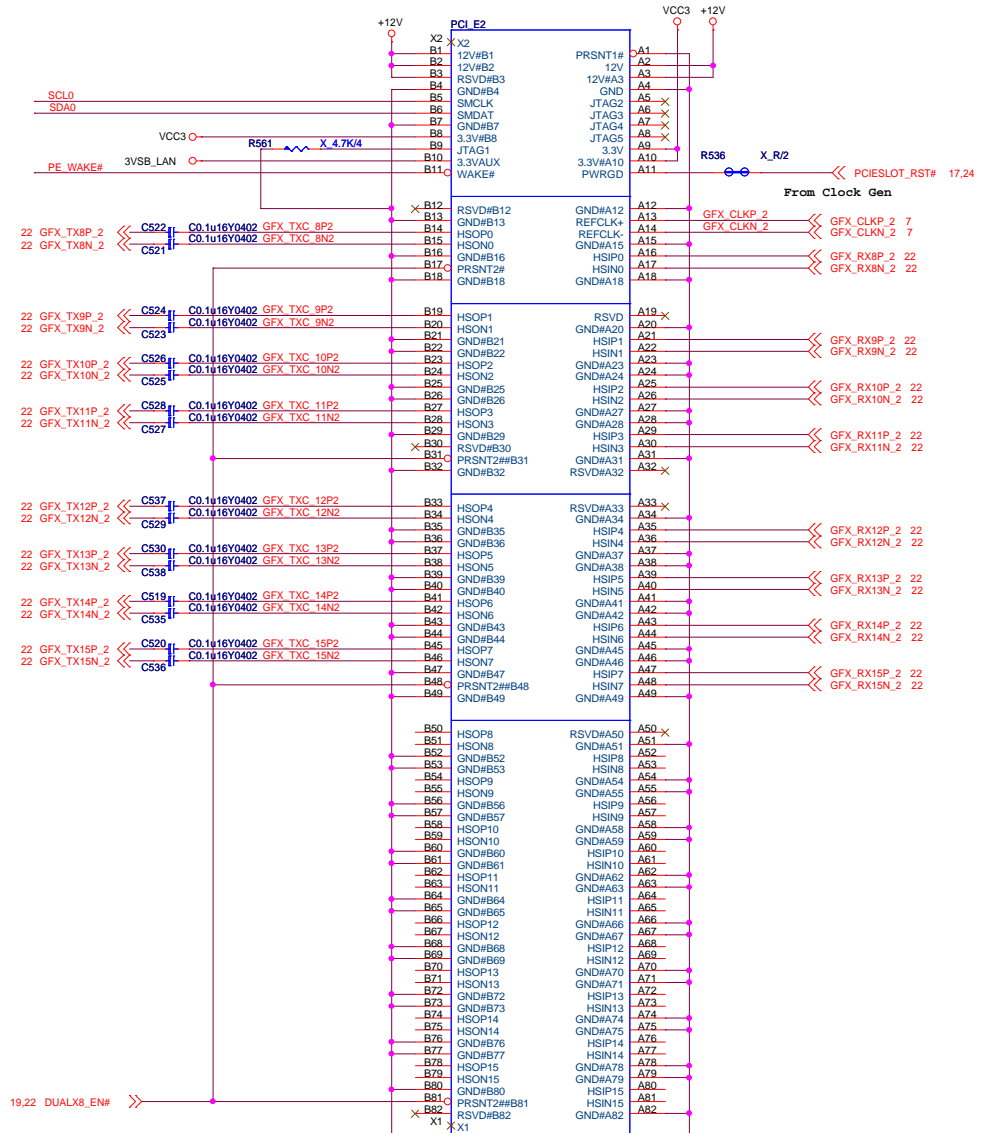


PCI EXPRESS x16 Slot



N11-1640401-K06

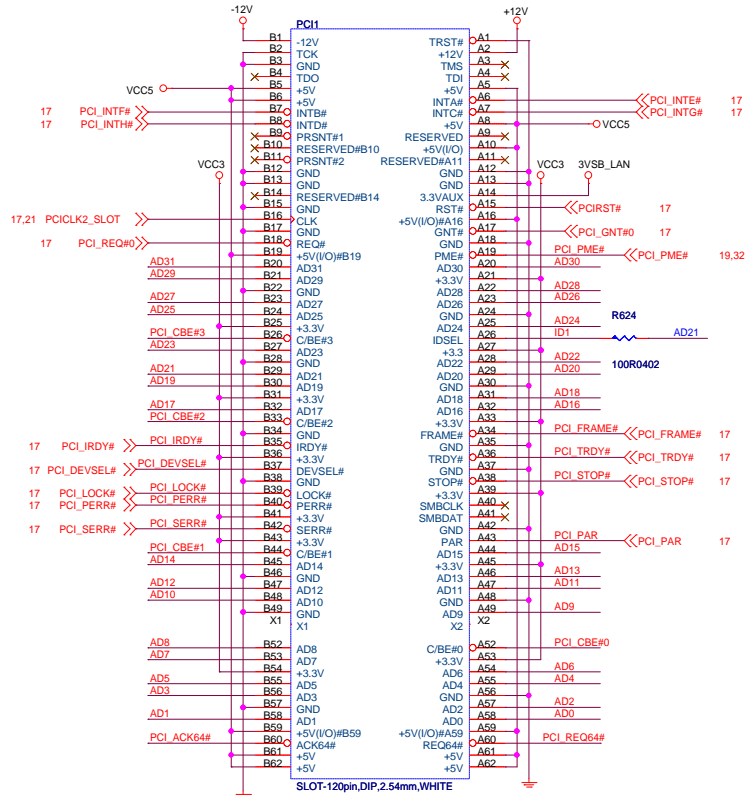
PCI EXPRESS x16 Slot



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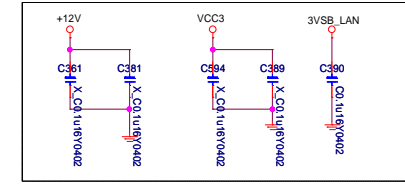
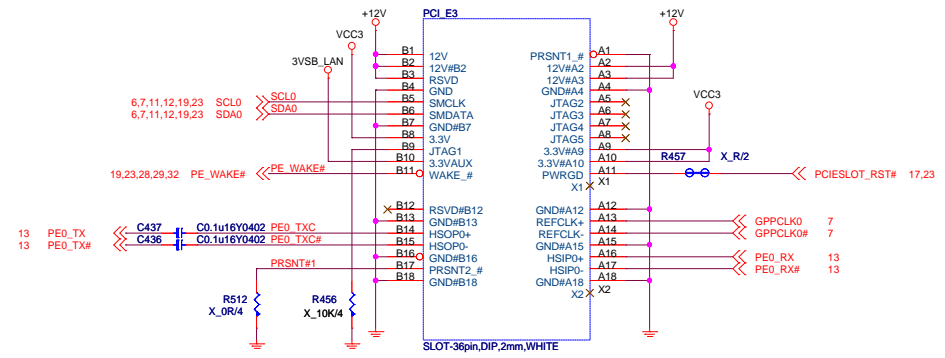
17 AD[31..0] >> AD[31..0]
17 PCI_CBE#[3..0] >> PCI_CBE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



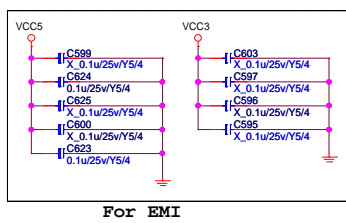
IDSEL = AD21
MASTER = PCI_REQ#0
PCI_GNT#0

PCI EXPRESS 1 Slot-1



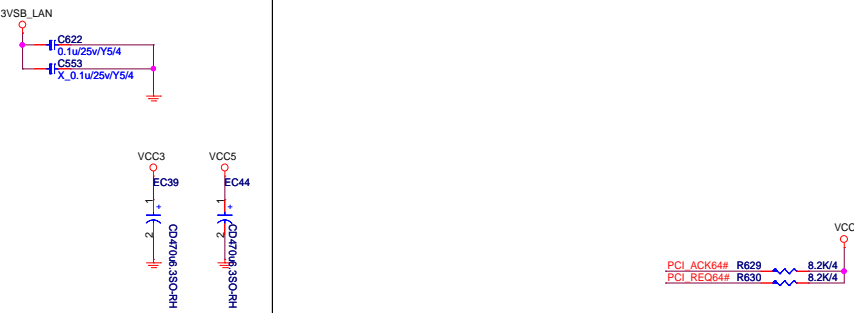
Placement Between at PCIe_X1

PCI SLOT DECOUPLING CAPACITORS

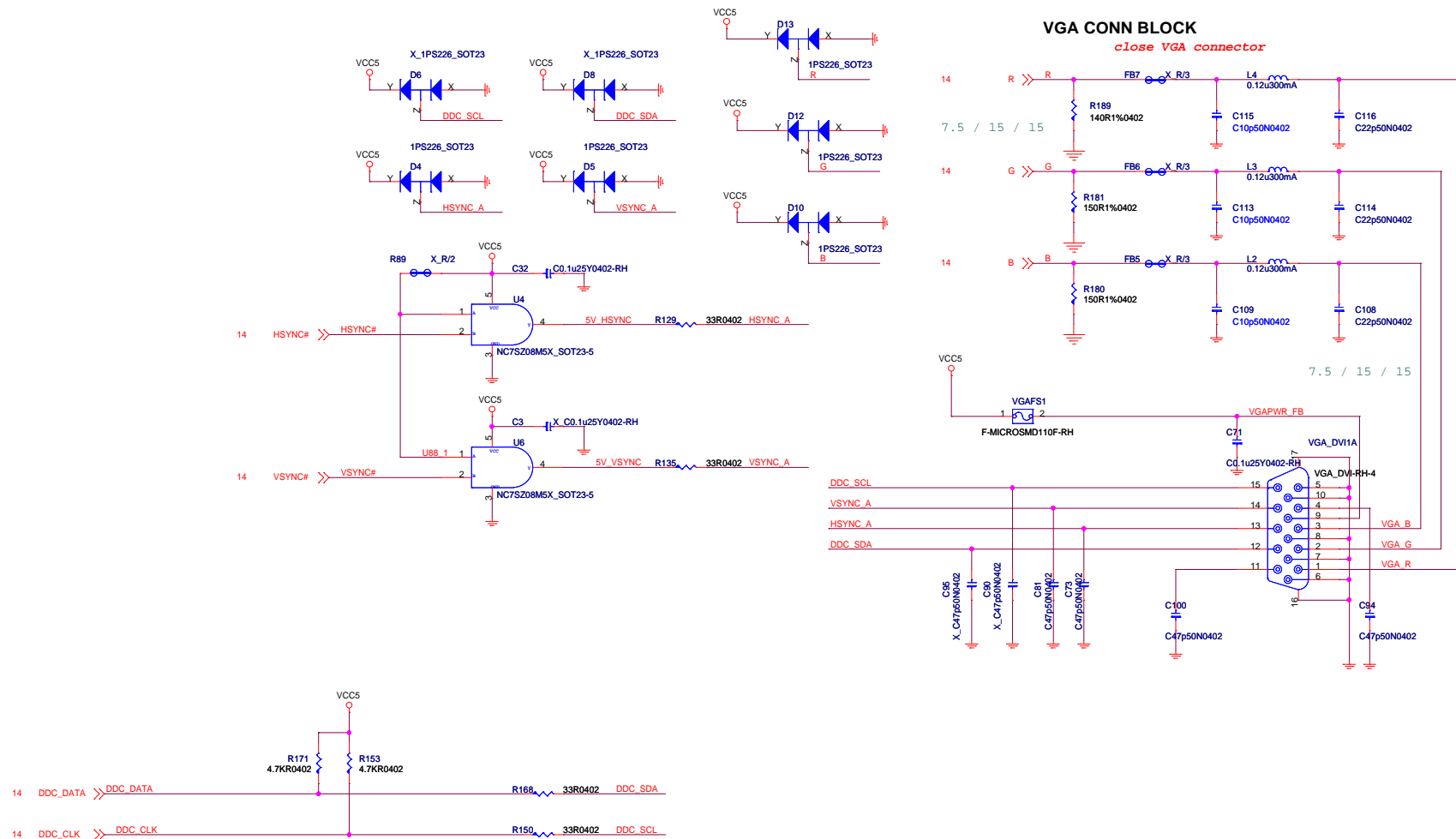


For EMI

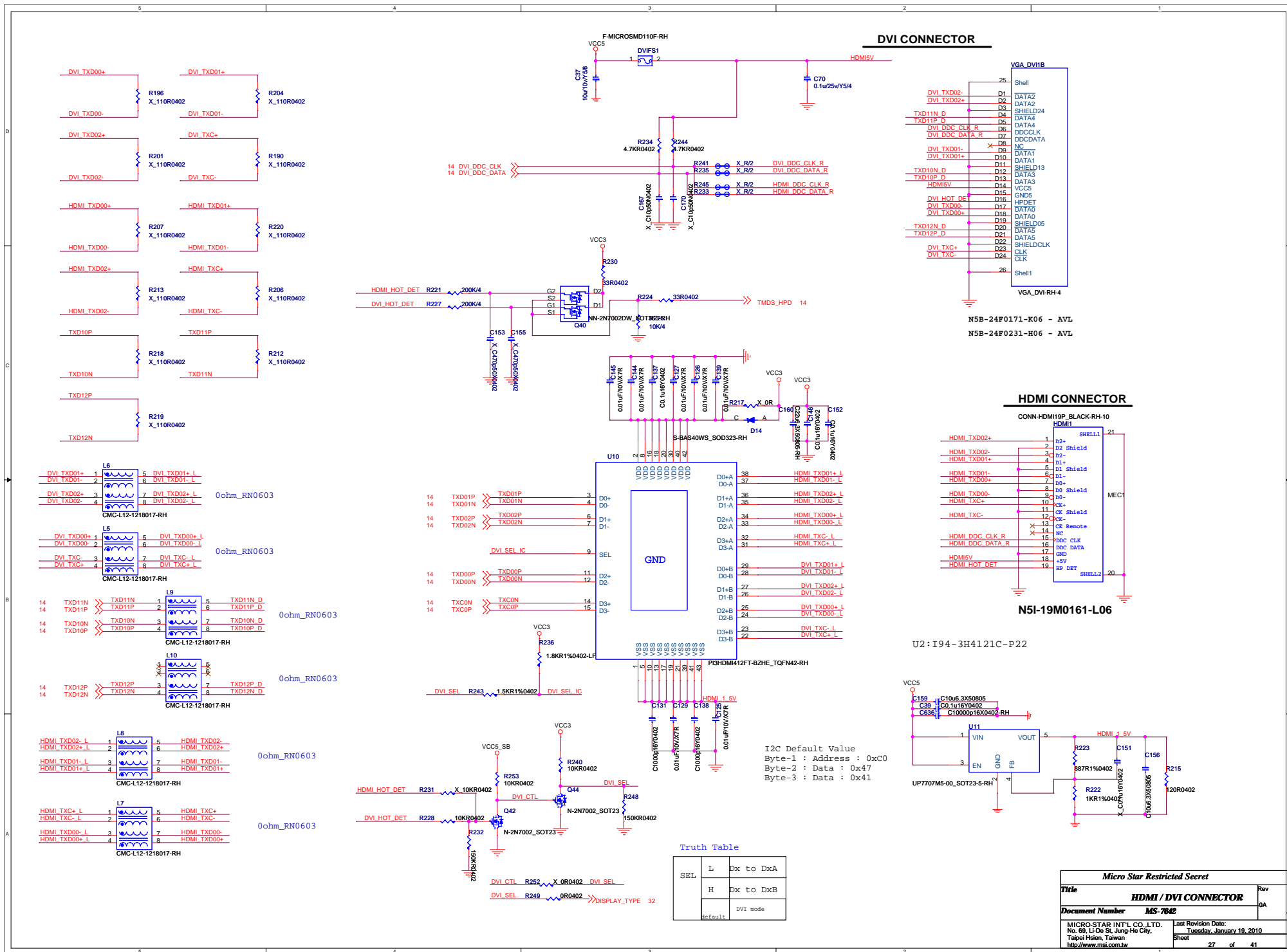
PCI PULL-UP / DOWN RESISTORS

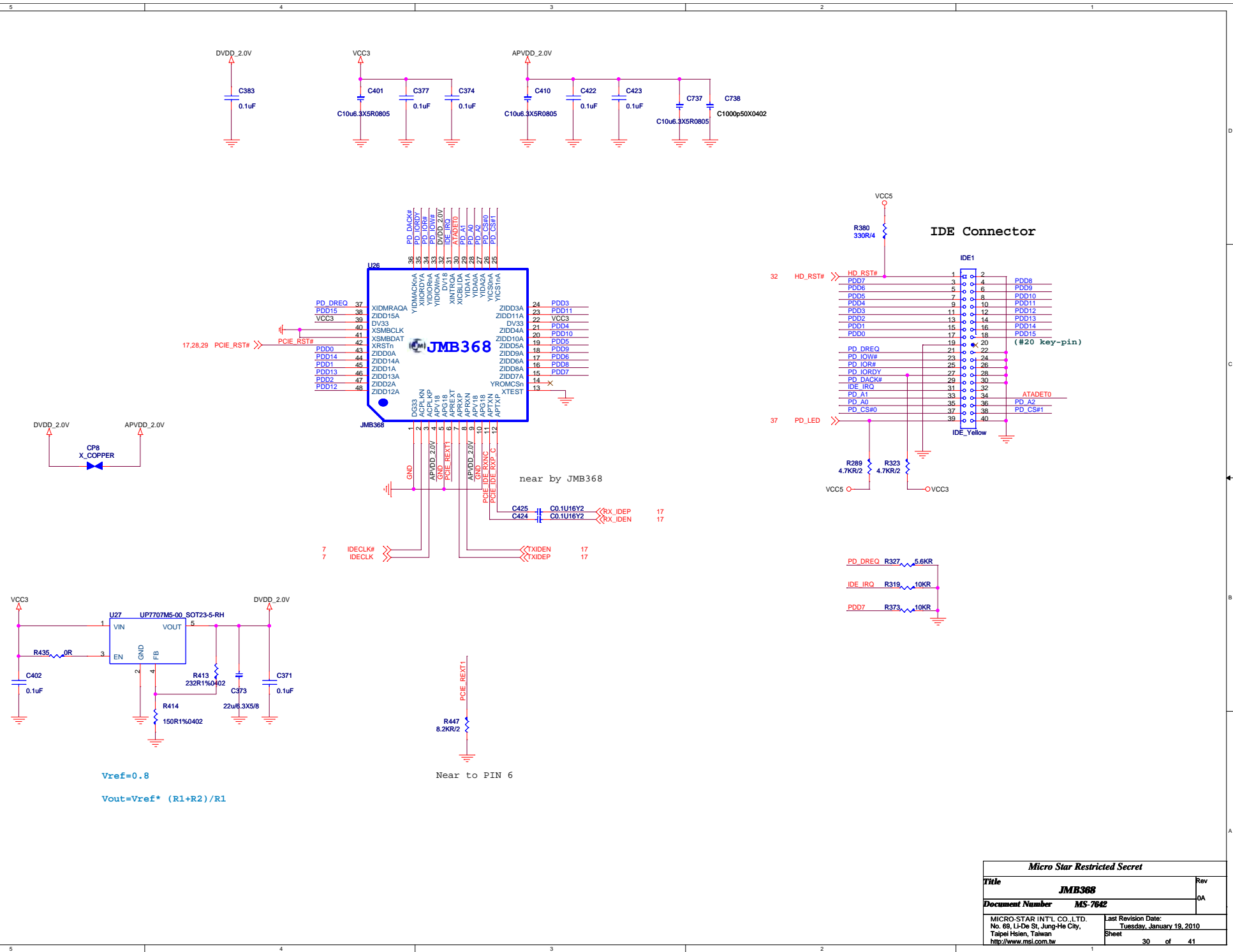


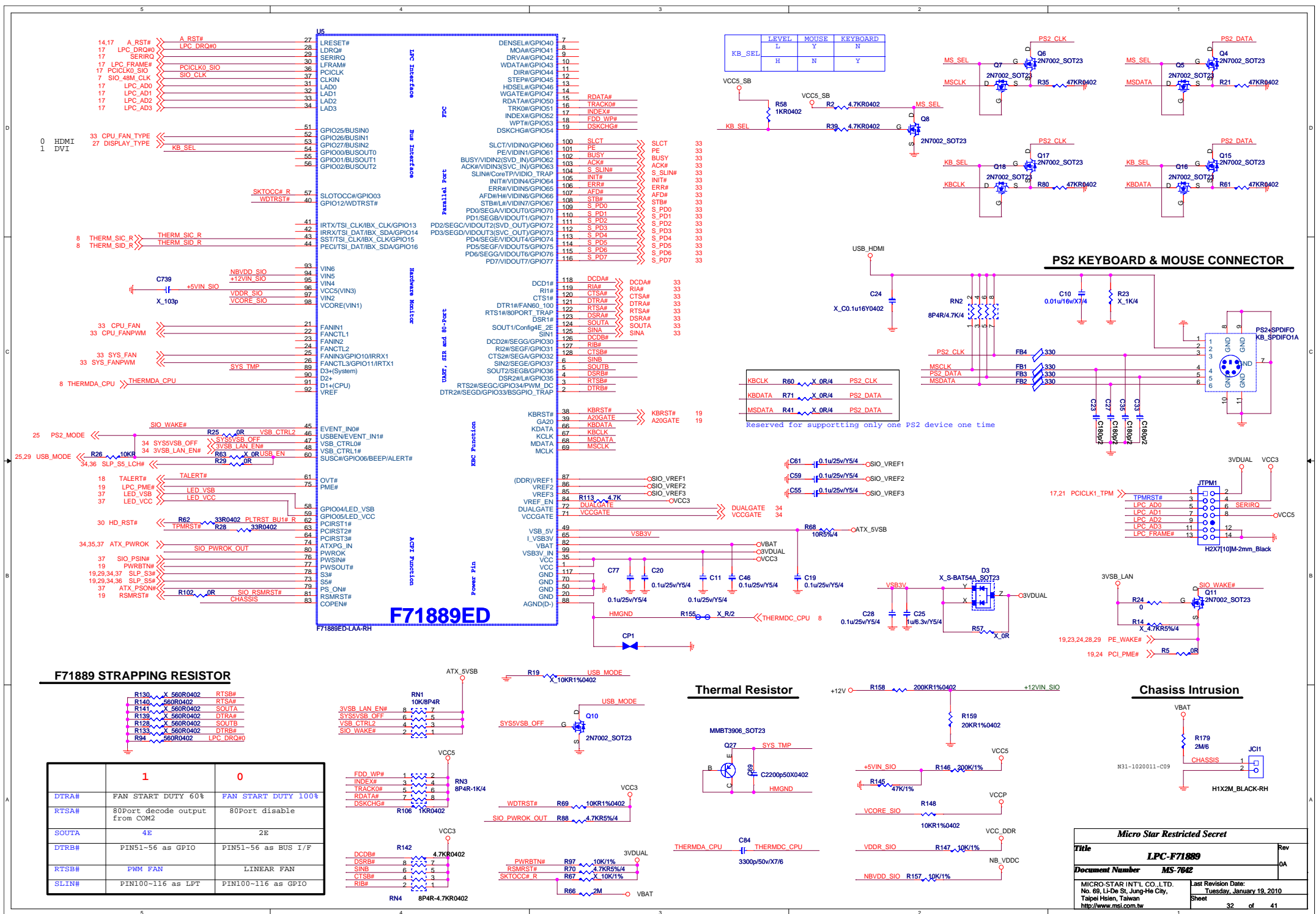
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D41
S-SM5817A

VCC5 ○ A C LPT VC

STB# R674 2.7KΩ402
RN8 8P4R-2.7KΩ402

S_PD3 1 2
S_PD2 3 4
S_SLIN# 5 6
INIT# 7 8
S_PD1 1 2
S_PD6 3 4
S_PD5 5 6
S_PD4 7 8

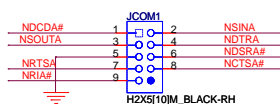
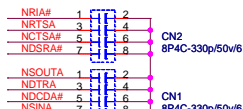
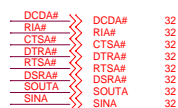
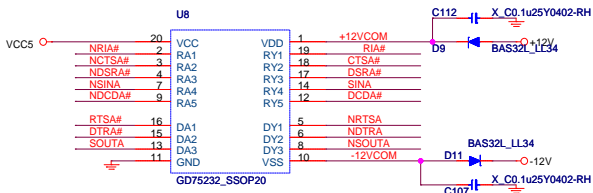
RN9
8P4R-2.7KΩ402

RN10 8P4R-2.7KΩ402

SLCT 1 2
PE 3 4
BUSY 5 6
ACK# 7 8
S_PD1 1 2
ERR# 3 4
S_PD0 5 6
AFD# 7 8

RN7 8P4R-2.7KΩ402

SLCT 32
PE 32
BUSY 32
ACK# 32
S_SLIN# 32
INIT# 32
ERR# 32
AFD# 32
STB# 32
S_PD0 32
S_PD1 32
S_PD2 32
S_PD3 32
S_PD4 32
S_PD5 32
S_PD6 32
S_PD7 32



FAN CONTROL

CPU FAN

32 CPU_FANPWM
32 SYS_FANPWM

12V

C52
0.1u/50v/X7/6

C54
0.1u/16v/Y5/4

C53
0.1u/50v/X7/6

Chirpmp -> 24 V

VCC3

R38
4.7K/4

32 CPU_FAN_TYPE

CPU_FAN_TYPE

U3
W83391TG

FAN1_IN
FAN2_IN
VCC12
C1
C2
CHRPMP
GND

FAN1_DRV
FAN1_SEN
FAN2_DRV
FAN2_SEN
FAN3_DRV
FAN3_SEN
FAN3_IN

Q9
N-APM2054NDC_SOT89

R54
10KR0402

R72
3.48K/6/1%

Q85
N-APM2054NDC_SOT89

R49
10KR0402

R45
3.48K/6/1%

D1
1N4148

R75
4.7KR0402

R109
27K/4

C47
X_1000p/50v/X7/4

R103
10KR0402

R12
4.7K/4

R11
200R/4

D2
1N4148

Q12
2N7002_SOT23

CPU_FANPWM

CPU_FAN_TYPE

CPUFAN
MEC1
BH1X4_White

SYSFAN

12V

D33
1N4148

R651
4.7KR0402

R650
27K/4

R657
10KR0402

C628
X_1000p/50v/X7/4

EC1
100u/16V/6.3*10.5/O

EC47
100u/16V/6.3*10.5/O

SYSFAN1
BH1X3_White

3
2
1

12V

R638
X_OR0805

12V

D33
1N4148

R651
4.7KR0402

R650
27K/4

R657
10KR0402

C628
X_1000p/50v/X7/4

EC1
100u/16V/6.3*10.5/O

EC47
100u/16V/6.3*10.5/O

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EC1
100u/16V/6.3*10.5/O

EC47
100u/16V/6.3*10.5/O

SYSFAN1
BH1X3_White

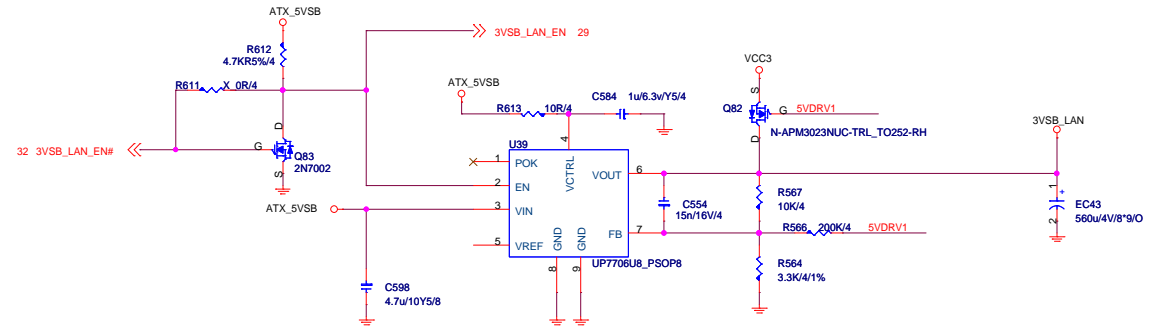
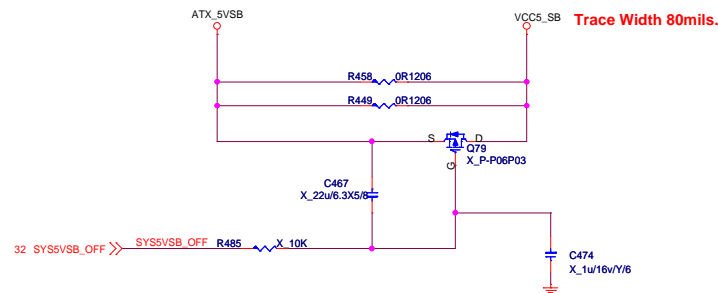
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12V

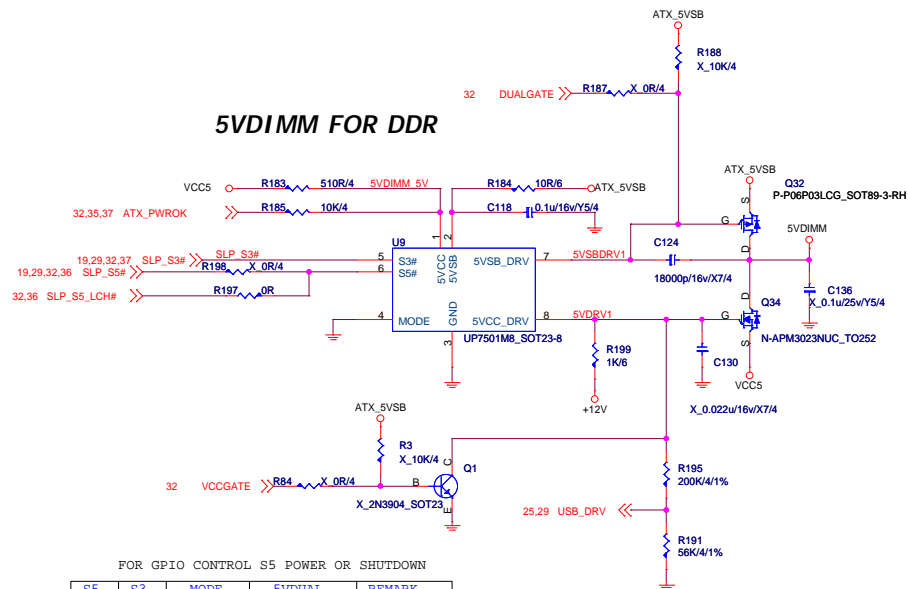
R638
X_OR080

Deep Mode WOL LAN Power CTRL Circuit

5VSB Power Switch

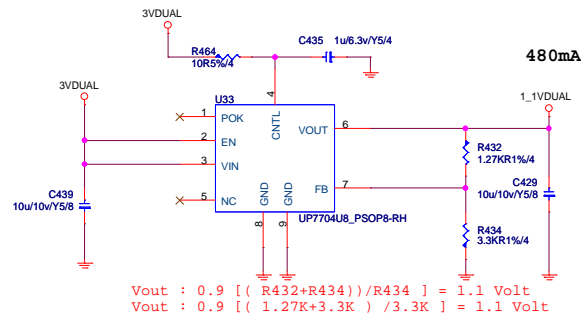
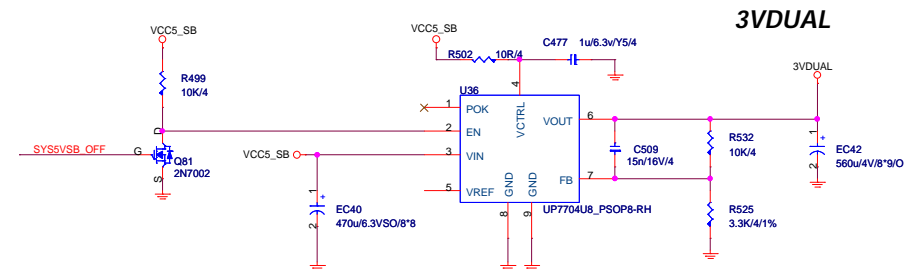
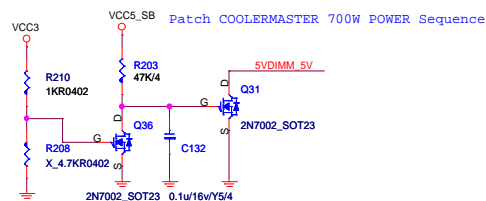


5V DIMM FOR DDR



FOR GPIO CONTROL S5 POWER OR SHUTDOWN

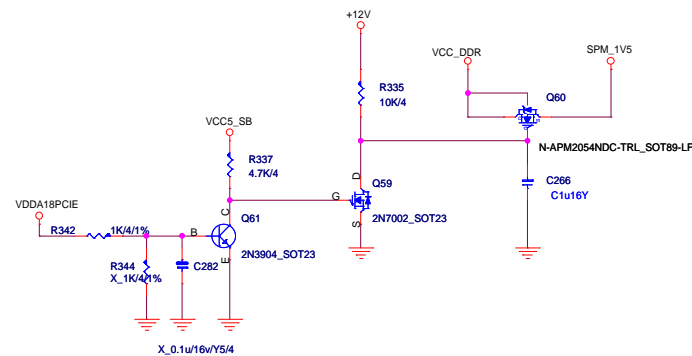
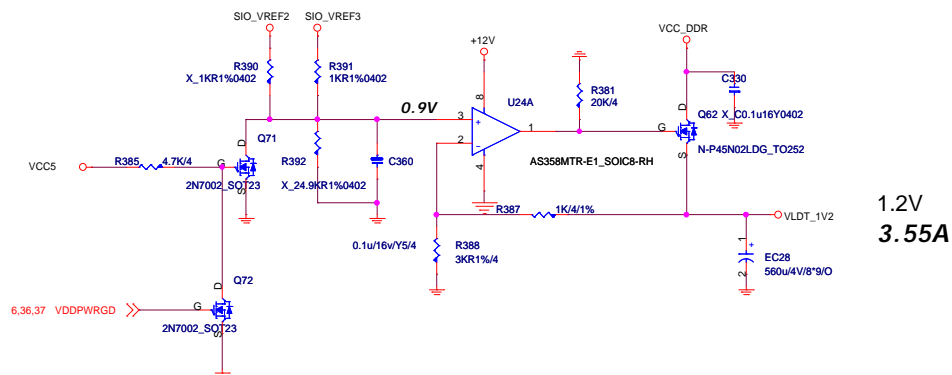
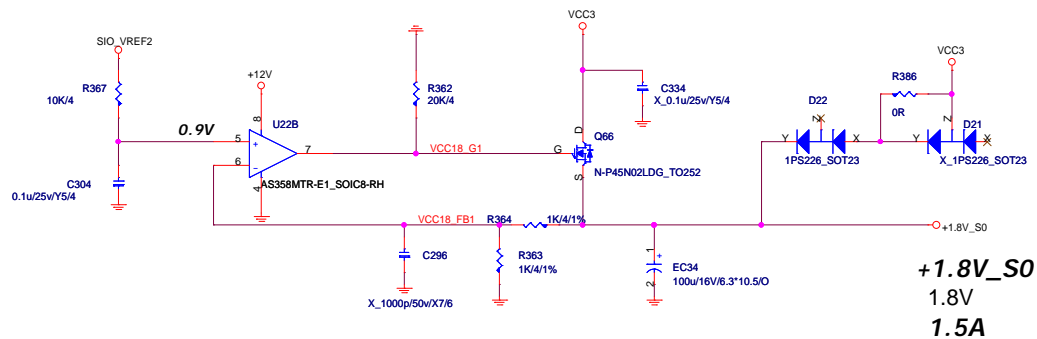
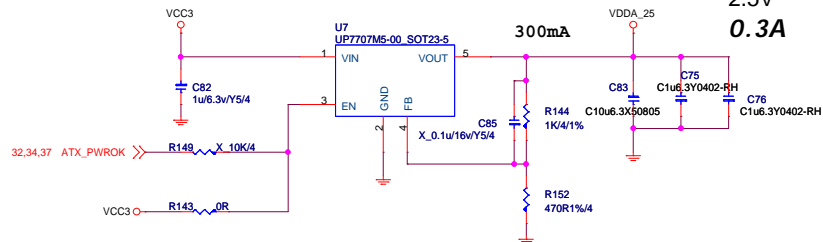
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1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWN	S4/S5



1P1V_SB_DUAL for SB, 480mA S0 - S5

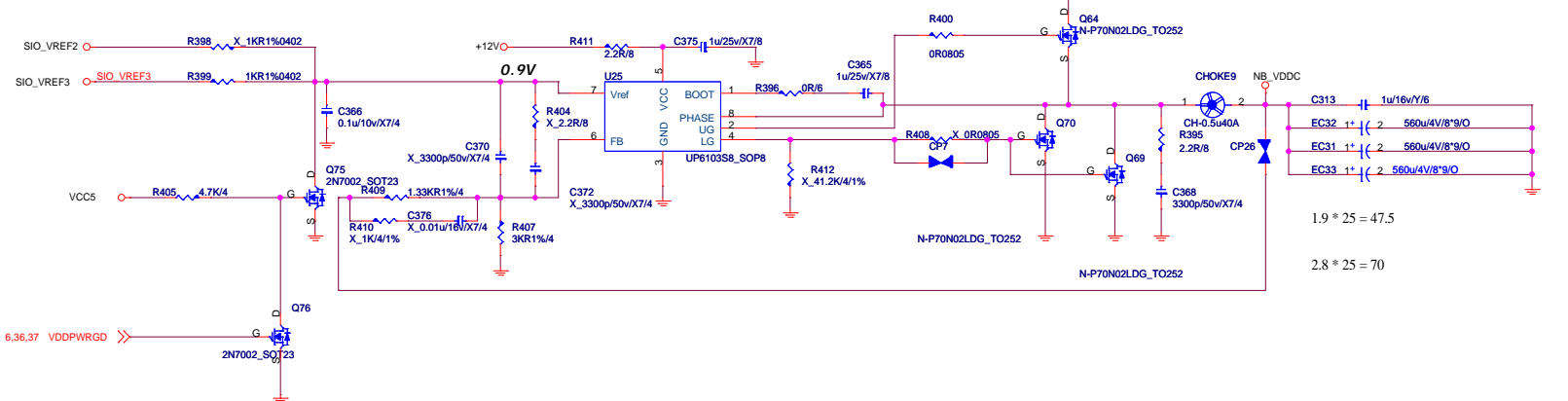
VDDA_25

2.5V
0.3A



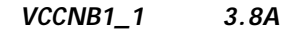
NB_VDDC

1.3V 25.8A



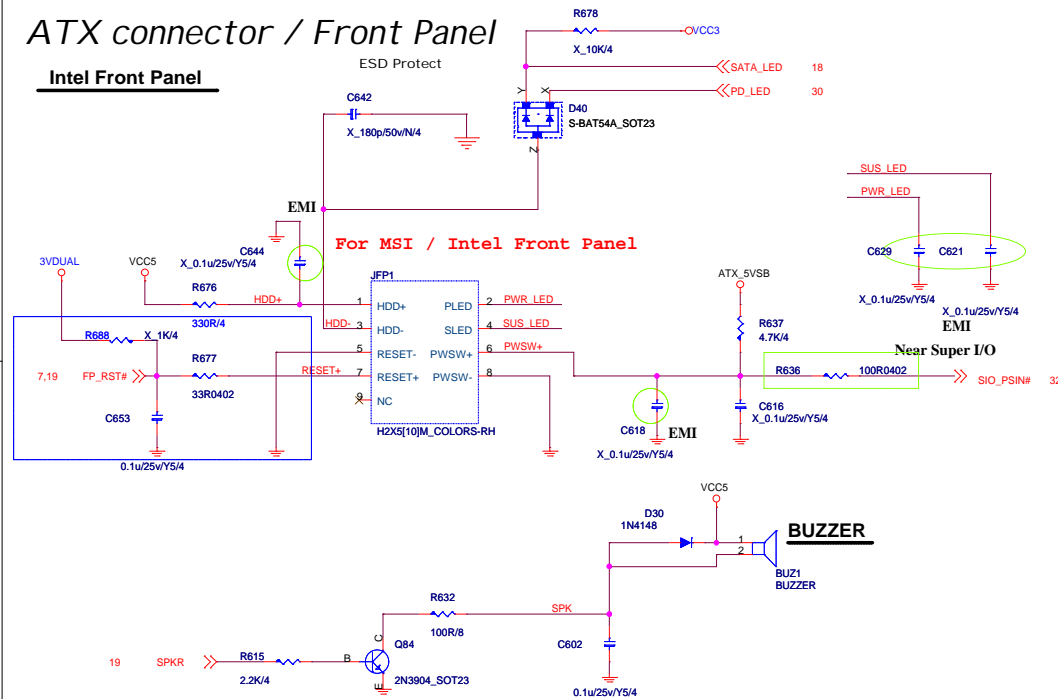
Micro Star Restricted Secret		
Title	UPI ACPI	Rev
Document Number	MS-7642	0A
MICRO-STAR INT'L CO., LTD. No. 69, L-Hsueh St., Jung-Hsi City, Taipei Hsien, Taiwan http://www.msi.com.tw		
Last Revision Date: Tuesday, January 19, 2010		
Sheet	35	of 41

VCC1_1 3.8A

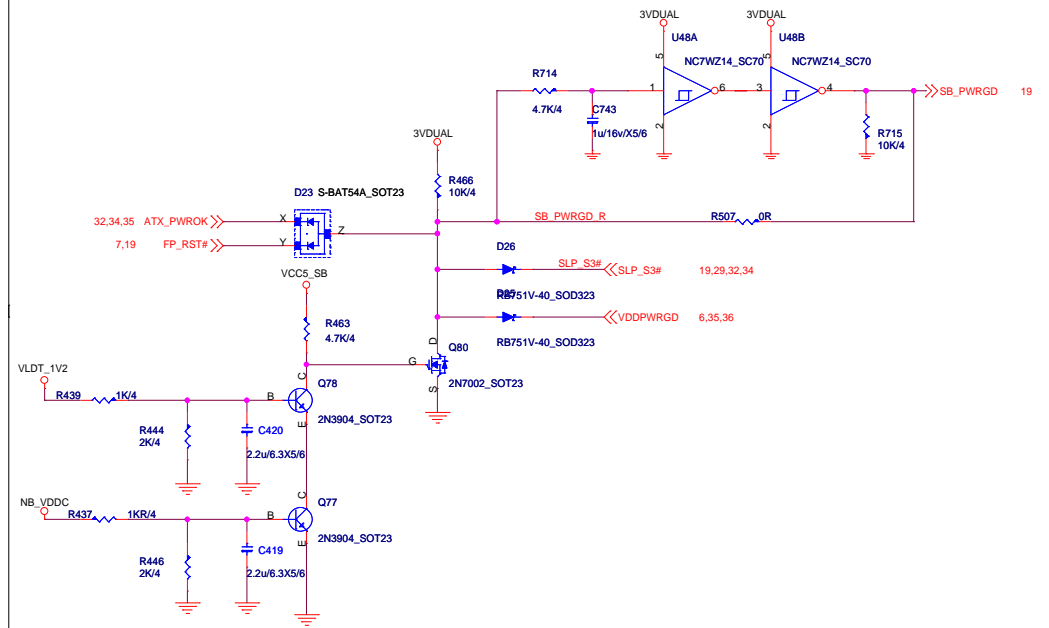
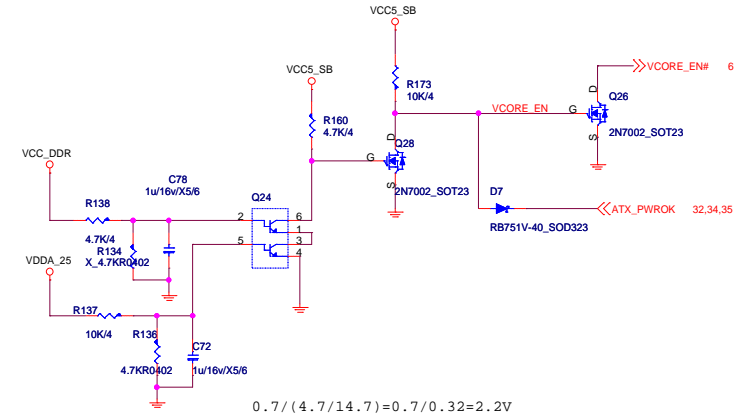
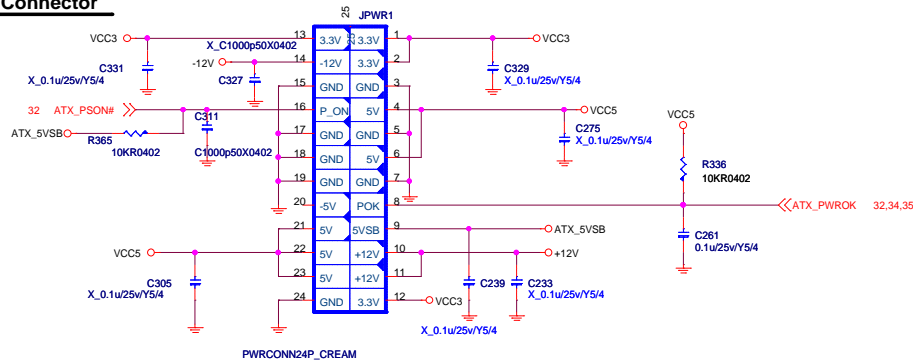


ATX connector / Front Panel

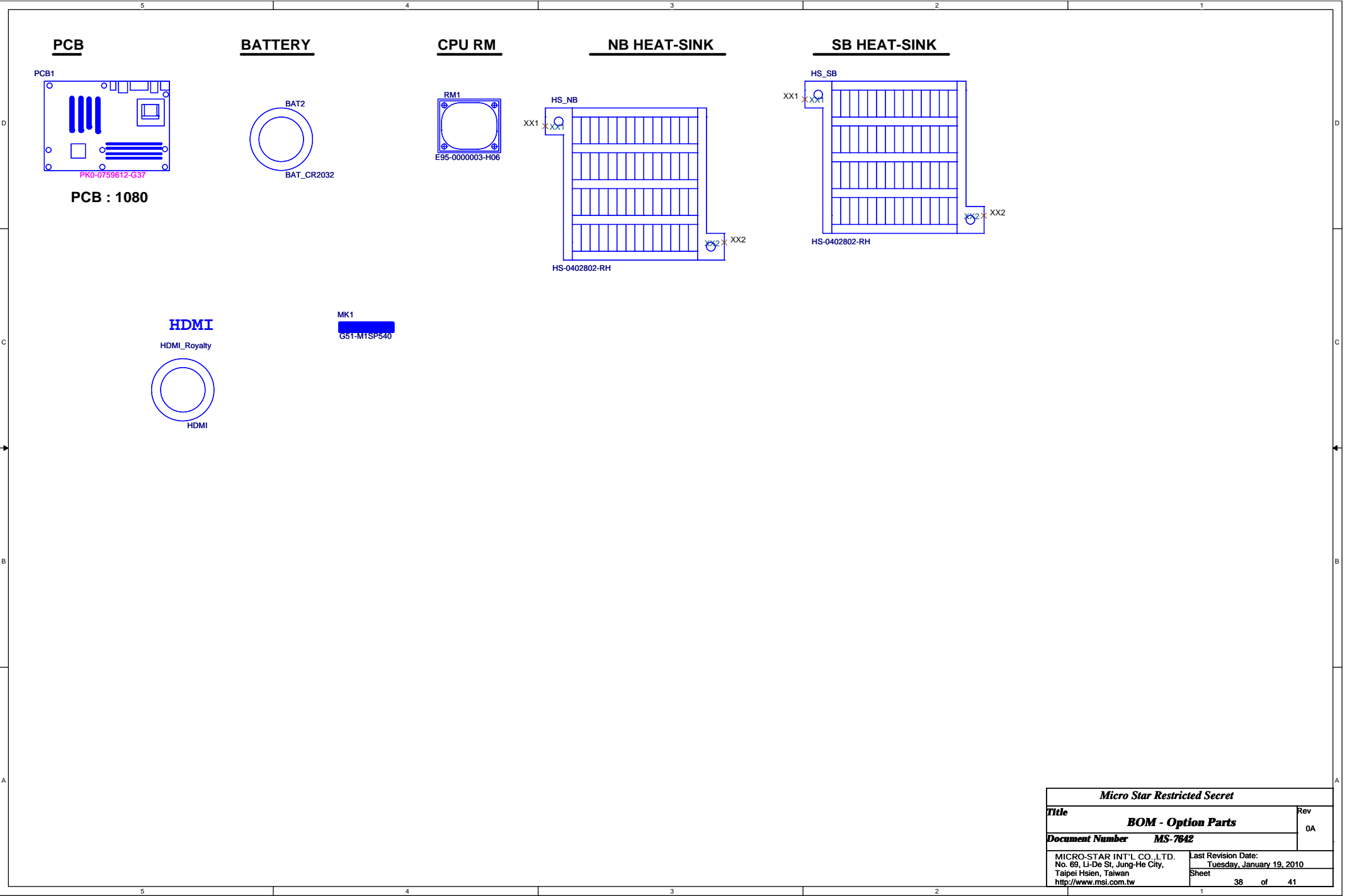
Intel Front Panel



ATX Connector



Micro Star Restricted Secret		
Title	ATX/Front Panel/KB/EMI	Rev
Document Number	MS-7642	0A
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St., Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		
Last Revision Date: Tuesday, January 19, 2010		
Sheet 37 of 41		



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Title	BOM - Option Parts
Document Number	MS-7642
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, January 19, 2010 Sheet 38 of 41

<i>Micro Star Restricted Secret</i>			
Title			Rev
PWROK MAP			0A
Document Number			
MS-7642			
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, January 19, 2010 Sheet <div style="display: flex; justify-content: space-between;"> 1 39 of 41 </div>	

5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				

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<i>Micro Star Restricted Secret</i>		
Title	RESET MAP	Rev
Document Number	MS-7842	0A
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, January 19, 2010
		Sheet 1 40 of 41

<i>Micro Star Restricted Secret</i>		
Title	HISTORY	Rev
Document Number	MS-7642	0A
MICRO-STAR INT'L CO., LTD. No. 68, Li-Huei St., Jung-Hsi City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, January 19, 2010 Sheet 41 of 41